**REMARKS**

Claims 1-16 are all the claims pending in the application.

I. Drawings

The Examiner requested corrected drawings in compliance with 37 CFR §1.121(D) to correct dark shading in figures 1-3. The Applicant is in the process of preparing the corrected drawings and will be submitting them separately in the near future.

II. Claim Rejections – 35 U.S.C. § 112

Claims 11 and 16 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicant respectfully traverses the rejection.

With regard to claim 11, the Examiner stated that the phrase "burst buffers" is not clearly explained in the specification or in the claim. Applicant disagrees with the Examiner, and submits that the phrase "burst buffers" is a term clearly explained in the specification and generally understood in the art. The idea of a buffer is well known in the field of communication and network nodes, and is described generally in paragraphs 3–5 of the Background of the Invention section of the present application. Since a buffer must, by definition, release stored data at some point, the "burst buffer" logically refers to a buffer that releases data in bursts. Applicant further cites to US Patent 5,557,266, to show that the term "burst buffer" is commonly used in the art without any need for specific explanation. See Col. 3, line 26 and line 40; Col. 4, line 36. The '266 patent, issued in 1996, makes general reference to a "burst buffer" at numerous points without specifically defining or identifying the term. Therefore, Applicant

contends that the term "burst buffer" is well known in the art and does not require additional explanation in the specification or claims.

In claim 16, the Examiner states that the term "*interactive cascaded* multi-channel network nodes" is also not clearly explained in the specification or claim. (emphasis by Examiner). Applicant has reviewed the specification and submits the term is properly explained in the application. Page 13, paragraph 2, of the application states "[i]n Fig. 3, the network node 10 incorporating an implementation example of cascaded memory queues is schematically shown." The arrangement of sequential memory queues is exemplary of the "cascaded" architecture of the network node described in the application. Furthermore, Applicant again cites to the '266 patent, which specifically discusses the use of a "cascading switch" without explicitly defining the term "cascading" in the specification. Col. 4, line 21-22. The additional modification of "interactive" is a literal definition of how the various components of the network node communicate and interact with each other. Therefore, Applicant submits that the term "interactive cascading multi-channel network node" does not require additional explanation in the specification or claims, and respectfully requests that the Examiner withdraw the rejection under 35 U.S.C. § 112.

III. Claim Rejections – 35 U.S.C. § 102

Claims 1, 2, 4-8 and 13-16 are rejected under 35 U.S.C. § 102(b) as being anticipated by Moriwaki et al (EP 0,918,419 A2; hereafter "Moriwaki").

Claim 1

With regard to independent claim 1, Applicant submits that Moriwaki does not disclose all of the features of the claimed invention. Specifically, Moriwaki does not disclose a "memory

unit organized as a number of physical memory queues, *each queue being assigned to an output port*." (emphasis added). For example, as shown in Figure 2 of the application, the memory unit 20 is arranged into memory queues 22 which "corresponds to the number of channels of the network node 10 and the output ports 34 of the switching unit 30, respectively." Page 10, para. 4. Further, "each output port 34 is assigned to a memory queue 22 of the memory unit," such that "each memory queue 22 is coupled with an output port 25 of the memory unit 20." Page 11, paras. 2-3. Therefore, the data that passes through a particular memory queue 22 must also be passed to a specific, assigned output port 25 of the memory unit 20.

In contrast, Moriwaki discloses a switching unit, and specifically a cell assembler and cell distributor, which does not assign specific queues to specific outputs. See Figs. 10 and 11. In the cell assembler, the memory queues 33 pass data into a demultiplexer 32, which then "distributes" data to any one output highway 50 that it chooses. See Moriwaki, Col. 12, lines 19-22. The aspect of claim 1 of the present application does not require a demultiplexer, as the memory queues are assigned to a specific output port.

The Examiner also refers to how the assembler of Moriwaki assigns cells having the same destination and eventually routes the cells to the same output line of a switch by a demultiplexer. However, this "assignment" of *cells* of data contrasts with claim 1, which assigns output ports to memory queues.

Therefore, as Moriwaki fails to disclose memory queues where each queue is assigned to an output port, Applicant submits that claim 1 is allowable over Moriwaki. Applicant respectfully requests that the rejection of claim 1 be withdrawn.

Further, as rejected claims 2-13 depend from claim 1, Applicant respectfully requests that the rejections on the remaining dependent claims be withdrawn as well.

Claim 2

With regard to claim 2, Applicant directs the Examiner to the arguments above with regard to claim 1. As Applicant submits that claim 1 is allowable over the cited prior art, and as claim 2 depends from claim 1, Applicant submits that claim 2 is also allowable.

Claim 4

With regard to claim 4, Applicant first disagrees that Moriwaki discloses the re-assembly unit coupled with input ports of the network node and the switching unit, as stated in claim 4. The Examiner cites to the input of a cell assembly unit of Moriwaki as being connected to the output of an ATM switch and relates this to the re-assembly unit of the claimed aspect. However, the re-assembly unit of the claimed aspect is connected with the input ports of the network node and the input ports of a switching unit, as further exemplified in Fig. 3. In contrast, the cell assembly unit of Moriwaki (see Fig. 1) is connected to the output of a switch 10-x and the output of the node 50-m, which serves a completely different function.

Applicant further disagrees that Moriwaki discloses a segmentation unit that is coupled with a memory unit and the output ports of the network node. The Examiner states that the dummy cell generator of Moriwaki "works as a segmentation unit to distribute the same number of cells in each switch." However, the present application states that the segmentation unit "segments the data and supplies it to a transmit unit 58," which is unrelated to the dummy cell generator located in the cell distributor of Moriwaki. In fact, the dummy cell generator 25 of Moriwaki is present in the cell distributor, which indirectly connects with data from an input port and feeds into a switch. In contrast, claim 4 of the present application specifically states that the segmentation unit is coupled with "output ports of the network node." Moriwaki does not

disclose that the dummy cell generator connects with the outputs of the network node, and Applicant therefore submits that Moriwaki does not anticipate claim 4.

Claim 5

With regard to claim 5, Applicant directs the Examiner to the arguments above with regard to claim 1. As Applicant submits that claim 1 is allowable over the cited prior art, and as claim 5 depends from claim 1, Applicant submits that claim 5 is also allowable.

Claim 6

The Examiner also states that Moriwaki clearly shows the elements of claim 6, wherein "said memory queues and said memory agents form said switching unit." However, the Examiner states that Moriwaki discloses an "ATM switch system comprising the cell distributor and the cell assembler that handles cells of ATM switches and place them into according memory queues." Applicant points out, however, that according to the quoted section of Moriwaki, it is the cell distributor and cell assembler that act as switches and place cells into memory queues, while in the aspect of claim 6 of the present application, it is the memory queues themselves that work with the memory agents to act as switches.

Therefore, for at least the reasons stated above, Applicant does not believe that Moriwaki discloses the elements of claim 6.

Claim 7

With regard to claim 7, Applicant directs the Examiner to the arguments above with regard to claim 1. As Applicant submits that claim 1 is allowable over the cited prior art, and as claim 7 depends from claim 5, which depends from claim 1, Applicant submits that claim 7 is also allowable.

Claims 8-10

With regard to claims 8-10, Applicant directs the Examiner to the arguments above with regard to claim 1. As Applicant submits that claim 1 is allowable over the cited prior art, and as claims 8-10 all depend from claim 1, Applicant submits that claims 8-10 are also allowable.

Claim 11

With regard to claim 11, Applicant does not believe that Moriwaki discloses a multi-channel network node with burst buffers. The Examiner cites to col. 13, lines 9-39 of Moriwaki, and states that the continuous transfer of data among inputs and outputs with little or no interruption operates as a burst buffer (in burst mode). However, Moriwaki never specifically states the use of a burst buffer, and the cited section of Moriwaki never states that the arrangement of queuing buffers in sequence does anything similar to a burst mode or a burst buffer. Moriwaki simply does not disclose a buffer that provides bursts of data. As a reference in a 35 USC §102(b) rejection must state each and every element of the recited claim, Applicant does not believe that the rejection of claim 11 is valid, since Moriwaki fails to disclose the specific use of a burst buffer.

Claim 12

With regard to claim 12, Applicant directs the Examiner to the arguments above with regard to claim 11 and claim 1. As Applicant submits that claim 11 and claim 1 are allowable over the cited prior art, and as claim 12 depends from claim 11, which depends from claim 1, Applicant submits that claim 12 is also allowable.

Claim 13

With regard to claim 13, Applicant directs the Examiner to the arguments above with regard to claim 1. As Applicant submits that claim 1 is allowable over the cited prior art, and as claim 13 depends from claim 1, Applicant submits that claim 13 is also allowable.

Claim 14

With regard to claim 14, Applicant refers the Examiner to the arguments presented above for claim 1. To restate, Applicant does not believe that Moriwaki discloses the specific step of "switching/routing data from the memory queues to the output port the respective memory queue *is assigned to*," as specifically stated in claim 14 (emphasis added). Moriwaki does not specifically assign memory queues to specific output ports, but instead uses a demultiplexer to decide where the data output from the memory queues is going to be sent. The aspect of the method of claim 14, in contrast, specifically assigns a memory queue to an output port. Therefore, Applicant does not believe that Moriwaki anticipates claim 14.

Claim 15

With regard to claim 15, Applicant directs the Examiner to the arguments above with regard to claim 14. As Applicant submits that claim 14 is allowable over the cited prior art, and as claim 15 depends from claim 14, Applicant submits that claim 15 is also allowable.

Claim 16

With regard to claim 16, Applicant directs the Examiner to the arguments above with regard to claim 14. As Applicant submits that claim 14 is allowable over the cited prior art, and as claim 16 depends from claim 14, Applicant submits that claim 16 is also allowable.

IV. Claim Rejections – 35 USC §103

Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Moriwaki in view of Li et al (US Patent 5,757,771; hereafter "Li"). Specifically, the Examiner stated that Moriwaki failed to disclose the memory unit where the memory queues are resizable in order to redistribute buffer capacity of the memory queues. The Examiner states that Li discloses an ATM switch that dynamically sets queue lengths, depending on different input data.

Applicant respectfully disagrees, and submits that while Li discloses memory queues of different lengths, Li fails to disclose the element of claim 3 - a memory cell that is *resizable* to re-distribute buffer capacity of the memory queues. Li makes no mention of the ability to *resize* a memory queue after the queue size has previously been chosen, and only discusses how the buffer memory is divided into sub-queues of a particular length necessary to hold data cells of a particular type. Li further states that once the memory queue lengths have been determined, they are given "prioritization rankings…so that data sub-queues having higher output rankings are sent out before data sub-queues having a lower output ranking." Col. 4, lines 24-26. If the memory queues were resizable, as in the aspect claimed in claim 3, there would be no need to rank the queues, since the queue sizes could be adjusted if the incoming data required it.

Therefore, Applicant submits that Li, in combination with Moriwaki, cannot be combined to disclose the ability to resize the number of memory cells in a memory queue, as in claim 3. Applicant respectfully requests that the rejection of claim 3 under 35 U.S.C. § 103(a) be withdrawn.

V. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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